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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/522,502	11/11/2005	Werner Ertle	I431.124.101/	1444

25281 7590 10/30/2008

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EXAMINER	
HUBER, ROBERT T	

ART UNIT	PAPER NUMBER
2892	

MAIL DATE	DELIVERY MODE
10/30/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/522,502	ERTLE ET AL.	
	Examiner	Art Unit	
	ROBERT HUBER	2892	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 July 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *18-41* is/are pending in the application.

4a) Of the above claim(s) *34-37* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *18-33 and 38-41* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 July 2008* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings were received on July 24, 2008. These drawings are accepted, and the objection stated in the previous office action is withdrawn.

Claim Objections

2. The amendments to claims 23, 26, 27, and 33 were received on July 24, 2008. The objection to claim 23 is withdrawn. Claims 26, 27, and 33 were amended to overcome the previous objections to the use of the term "*adapted*". The objections to claims 26, 27, and 33 are withdrawn. However, as noted below, the use of the phrase "*a width determined in response to*" in claims 26 and 33 is a product by process limitation, and is not given patentable weight (See MPEP 2113).

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

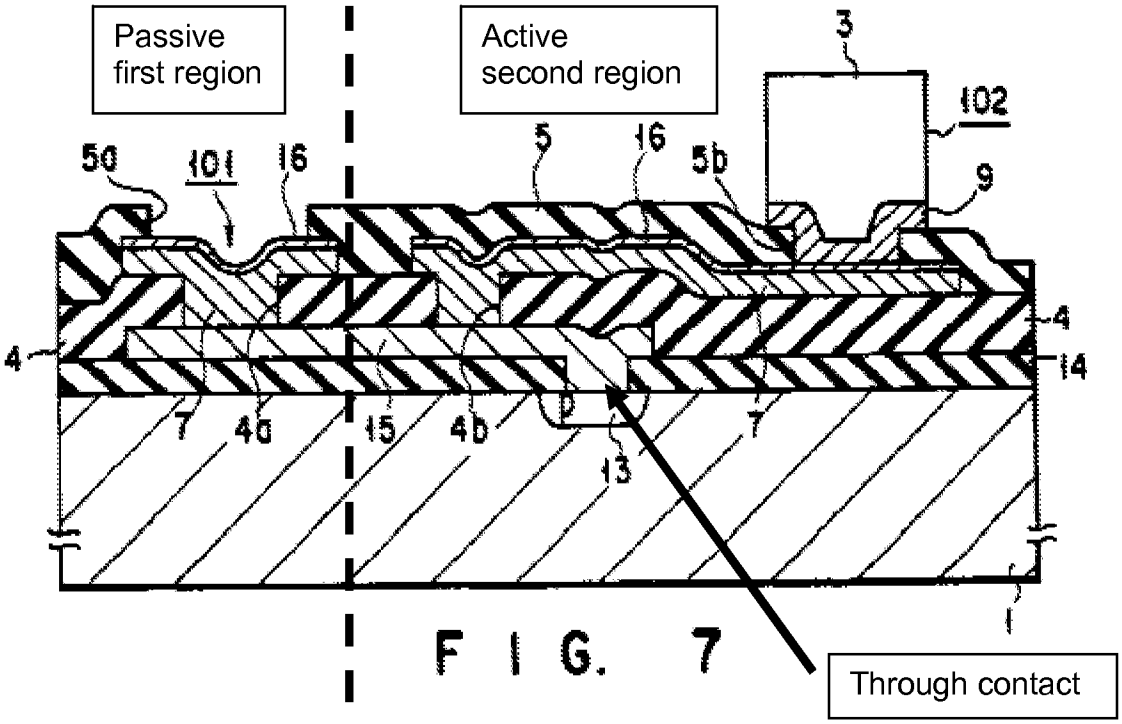
4. Claims 18 - 21, 23, 24, 26, 27, and 38 - 41 are rejected under 35 U.S.C. 102(e) as being anticipated by Yoshida (US 6,445,001 B2).

a. Regarding claim 18, **Yoshida discloses a semiconductor chip** (shown in figure 7) **comprising:**

a passive first region on a top side of the semiconductor chip (first region of the chip contain all the components to the left of the number "**15**". See figure below.);

an active second region on the top side of the semiconductor chip (second region of the chip containing all the components to the right of the number "**15**". See figure below.);

an arrangement of contact areas and test areas which are in each case electrically conductively connected to one another (contact areas and test areas comprising the components 7, 16, and 9, which are electrically connected to one another through electrode 15), **the contact areas being arranged in the passive first region** (contact areas 7 and 16 in the passive region), **the passive first region having no components of an integrated circuit** (as seen in figure 7, there are no components of an integrated circuit in the passive region), **the test areas being arranged in the active second region** (test areas 7, 16, and 9 in the active region), **the active second region having components of an integrated circuit** (second region has the active components of a diode, due to the p -type implant 13 and the n-type substrate 1, disclosed in col. 5, line 59).



F I G. 7

b. Regarding claim 19, **Yoshida discloses the semiconductor chip of claim 18, as cited above, comprising at least one electrically insulating layer** (layer 4) **comprising silicon dioxide and/or silicon nitride** (silicon dioxide, disclosed in col. 6, line 2) **arranged between the components of an integrated circuit and the test areas of the semiconductor chip** (as seen in figure 7).

c. Regarding claim 20, **Yoshida discloses the semiconductor chip of claim 18, as cited above, comprising wherein the contact areas and the test areas are electrically conductively connected via a conduction web** (conduction web comprising leads 15).

d. Regarding claim 21, **Yoshida discloses the semiconductor chip of claim 20, as cited above, comprising wherein through contacts through an insulating layer are arranged in the region of the conduction web, the through contacts being connected to interconnects to the electrodes of the components of the integrated circuit** (through contacts extending from web layer 15 to p-type implant 13 (see above figure), through insulating layer 14, disclosed in col. 5, line 60).

e. Regarding claim 23, **Yoshida discloses the semiconductor chip of claim 20, as cited above, comprising wherein the contact areas and the test areas at their edges and the conduction web on its top side have a multilayer insulation and passivation layer** (multilayer insulation and passivation layer comprising layers 4 and 5, as seen on the top side of the conduction web and on the edges of the test and contact areas in figure 7).

f. Regarding claim 24, **Yoshida discloses the semiconductor chip of claim 23, comprising wherein the multilayer insulation and passivation layer includes a silicon dioxide layer arranged directly on the edges of the contact areas and of the test areas and on the connecting conduction web** (layer 5 is directly arranged at the edges of the contact and test areas, which includes silicon dioxide, as disclosed in col. 6, line 13).

g. Regarding claim 26, **Yoshida discloses the semiconductor chip of claim 20, as cited above, comprising wherein the conduction web is formed in T having a transverse bar and a longitudinal bar, the transverse bar of the T having a width about equal to the width of the contact areas and having through contacts to interconnects, while the longitudinal bar of the T has a width determined in response to the maximum current loading during testing by test tips** (as seen in figure 7, the conduction web has the shape of a T, with the transverse bar 15 of the T about equal in width (vertical width) to that of the contact area, which is formed by layers 7 on layer 4, and comprises through contacts in regions such as denoted by 4b. The longitudinal bar, extending from layer 4, through layer 14, and to p-type implant 13, has a width determined in response to maximum current loading during testing since the device made for die testing, as disclosed in col. 3, lines 6 – 11. Furthermore, the claim limitation of "*a width determined in response to the maximum current loading*" is not given patentable weight since the patentability of a product does not depend on the method of production. See MPEP 2113.)

h. Regarding claim 27, **Yoshida discloses the semiconductor chip of claim 18, as cited above, comprising wherein the test areas have a width (b_p) about equal to a width of the contact areas and have a length (l_p) greater than their width (b_p)** (as seen in figures 6 and 7, the width of the test

areas are about equal to the width of the contact areas, and the length of the test area is greater than its width).

i. Regarding claim 38, **Yoshida discloses a semiconductor wafer** (figure 6) **comprising:**

a plurality of semiconductor chips (wafer in figure 6 has a plurality of semiconductor chips, which are individually show in figure 7) **having a passive first region** (first region of the chip contain all the components to the left of the number "**15**". See figure above.) **and an active second region** (second region of the chip containing all the components to the right of the number "**15**". See figure above.), **the semiconductor chips having an arrangement of contact areas and test areas which are electrically conductively connected to one another** (contact areas and test areas comprising the components 7, 16, and 9, which are electrically connected to one another through electrode 15);

the contact areas being arranged in the passive first region of the top side of the semiconductor chip (contact areas 7 and 16 in the passive region, which is on the top side of the semiconductor chip, as seen in figure 7), **the passive first region having no components of an integrated circuit** (as seen in figure 7, there are no components of an integrated circuit in the passive region); **and**

the test areas being arranged in the active second region of the top side of the semiconductor chip (test areas 7, 16, and 9 in the active region,

which is on the top side of the semiconductor chip, as seen in figure 7), **the active second region having components of an integrated circuit** (second region has the active components of a diode, due to the p -type implant 13 and the n-type substrate 1, disclosed in col. 5, line 59).

j. Regarding claim 39, **Yoshida discloses a semiconductor chip** (figure 7) **comprising:**

a passive first region on a side of the semiconductor chip (first region on the left side of the chip contain all the components to the left of the number "**15**". See figure above.);

an active second region on the side of the semiconductor chip (second region on the right side chip containing all the components to the right of the number "**15**". See figure above.)**;**

an arrangement of contact areas and test areas which are in each case electrically conductively connected to one another (contact areas and test areas comprising the components 7, 16, and 9, which are each electrically connected to one another through electrode 15)**, the contact areas being arranged in the passive first region** (contact areas 7 and 16 in the passive region)**, the passive first region having no components of an integrated circuit** (as seen in figure 7, there are no components of an integrated circuit in the passive region)**, the test areas being arranged in the active second region** (test areas 7, 16, and 9 in the active region)**, the active second region**

having components of an integrated circuit (second region has the active components of a diode, due to the p -type implant 13 and the n-type substrate 1, disclosed in col. 5, line 59).

k. Regarding claim 40, **Yoshida discloses the semiconductor chip of claim 18, as cited above, comprising at least one electrically insulating layer means comprising silicon dioxide and/or silicon nitride arranged between the components of an integrated circuit and the test areas of the semiconductor chip** (as seen in figure 7, insulating layer 4, disclosed in col. 6, line 2 as being made of silicon dioxide, is arranged between the components of the integrated circuit and the test areas of the semiconductor chip).

l. Regarding claim 41, **Yoshida discloses the semiconductor chip of claim 18, as cited above, wherein each of the contact areas is electrically conductively connected to a respective one of the test areas by a conduction web extending between and in the same plane as the contact area and the respective test area** (e.g. as seen in figure 7, contact areas comprise layers 7 and 16 in the passive first region, and test areas comprise layers 7, 16, and 9 in the active second region, as clarified in the figure above. The conduction web comprising layers 15 and 7 extending between the first and second active region and electrically connecting the two areas, wherein layer 7 of the conduction web is in the same plane as the contact and test areas).

Claim Rejections - 35 USC § 103

5. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 28, 29, and 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yoshida.

a. Regarding claim 28, **Yoshida discloses an electronic device comprising** (see figure 6):

a semiconductor chip (see figure 16, which relates to figures 6 and 7, by adding an additional interconnect layer, disclosed in col. 8, lines 42 - 45), **the semiconductor chip having an arrangement of contact areas and test areas**

which are in each case electrically conductively connected to one another (contact areas and test areas comprising the components 7, 16, and 9), **the contact areas being arranged in a passive, first region of the top side of the semiconductor chip** (first region of the chip contain all the components to the left of the p-type implant 13)**, the passive first region having no components of an integrated circuit** (as seen in figure 16, there are no components of an integrated circuit in the passive region)**;**

the test areas being arranged in an active, second region of the top side of the semiconductor chip (second region of the chip contain all the components to right side, including the p-type implant 13.)**, the active second region having components of an integrated circuit** (second region has the active components of a diode, due to the p -type implant 13 and the n-type substrate 1, disclosed in col. 5, line 59)**;**

test areas and contact areas being formed in the same interconnect plane (as seen in figures 7 and 16, the contact and test areas are in the same interconnect plane); **and**

Yoshida is silent with respect to explicitly stating that the length (l_p) of the test areas being at least approximately 1.5 times greater than the width (b_p) thereof. However, as seen in figures 6 and 16, the length of the test areas are at least approximately 1.5 times greater than their width. Although the figures are not indicated to be drawn to scale, it would have been obvious for one of ordinary skill in the art at the time the invention was made to

make the structure of Yoshida such a that the length of the test areas are at least approximately 1.5 times greater than their width, since the figures imply such a configuration for the device. Furthermore it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only ordinary skill in the art. *In re Aller*, 105 USPQ 233. One would have been motivated to make such a modification in order to accommodate the more chips on the periphery of the device, as indicated in figure 6.

b. Regarding claim 29, **Yoshida further discloses the electronic device of claim 28, as cited above, the semiconductor chip further comprising:**

at least one electrically insulating layer comprising silicon dioxide and/or silicon nitride arranged between the components of an integrated circuit and the test areas of the semiconductor chip (insulating layer 5, made of silicon dioxide, disclosed in col. 6, line 13),

wherein the contact areas and the test areas are electrically conductively connected via a conduction web (conduction web 15),

and wherein through contacts through an insulating layer are arranged in the region of the conduction, the through contacts being connected to interconnects web (through contacts extending from web layer 15 through insulating layer 14 to interconnect 21) **to the electrodes of the components of the integrated circuit** (interconnects 21 are connected to the

electrodes of the component of the integrated circuit, which is the diode of the p-type implant 13 and the n-type substrate 1).

c. Regarding claim 33, **Yoshida further discloses the semiconductor chip of claim 29, as cited above, comprising wherein the conduction web is formed in T having a transverse bar and a longitudinal bar, the transverse bar of the T having a width about equal to a width of the contact areas and having through contacts to interconnects, while the longitudinal bar of the T has a width determined in response to the maximum current loading during testing by test tips** (as seen in figure 16, the conduction web has the shape of a T, with the transverse bar15 of the T about equal in width (vertical width) to that of the contact area, which is formed by layers 7 on layer 4, and comprises through contacts in regions such as those in the middle of the figure. The longitudinal bar, extending from layer 4, through layer 14, and to interconnect 21, has a width determined in response to maximum current loading during testing since the device made for die testing, as disclosed in col. 3, lines 6 – 11. Furthermore, the claim limitation of "*a width determined in response to the maximum current loading*" is not given patentable weight since the patentability of a product does not depend on the method of production. See MPEP 2113).

8. Claims 22, 25, and 30 – 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yoshida in view of Henson (US 6,133,054).

b. Regarding claims 22 and 30, **Yoshida discloses the semiconductor chip of claim 21 and 29, as cited above respectively, but is silent with respect to the interconnects to the electrodes of the components of the integrated circuit comprise copper or a copper alloy. Henson discloses that interconnects to electrodes of components of an integrated circuit may comprise copper** (e.g. figure 7 shows interconnects 712 and 718, which can comprise copper or copper alloys, as disclosed in col. 4, lines 16 - 23).

It would have been obvious for one of ordinary skill in the art at the time the invention was made to use copper for the material of the interconnect structure of Yoshida since it was well-known in the art that copper can be used for interconnects in test circuits for integrated circuits, as disclosed by Henson. Furthermore, it has been held by the courts that selection of a prior art material on the basis of its suitability for its intended purpose is within the level of ordinary skill. *In re Leshing*, 125 USPQ 416 (CCPA 1960) and *Sinclair & Carroll Co. v. Interchemical Corp*., 65 USPQ 297 (1945). One would have been motivated to use copper as an interconnect structure since is a low-resistance conductor that is relatively inexpensive.

c. Regarding claim 25, **Yoshida discloses the semiconductor chip of claims 23, as cited above, but is silent with respect to the multilayer insulation and passivation layer comprises a silicon nitride layer and a polyimide layer. Henson discloses that a multilayer insulation and**

passivation layer may comprise silicon nitride and a polyimide layer (e.g. figure 7 shows multilayer insulation and passivation layers 722 and 724. col. 4, lines 22 - 23 disclose that layer 722 may be silicon oxynitride, which comprises silicon nitride, and col. 4, lines 52 – 53 discloses that layer 24 may be a polyimide layer).

It would have been obvious for one of ordinary skill in the art at the time the invention was made to use polyimide and silicon nitride for the materials of the multilayer insulation and passivation layer for the device of Yoshida since it was well-known in the art that such materials for layers can be used in test circuits for integrated circuits, as disclosed by Henson. Furthermore, it has been held by the courts that selection of a prior art material on the basis of its suitability for its intended purpose is within the level of ordinary skill. *In re Leshing*, 125 USPQ 416 (CCPA 1960) and *Sinclair & Carroll Co. v. Interchemical Corp.*, 65 USPQ 297 (1945). One would have been motivated to use silicon nitride and a polyimide as layers in a multilayer insulation and passivation layer since silicon nitride has well known properties of insulation and is easily manufactured, and polyimide layers are thermally stable and chemically resistant.

d. Regarding claim 31, **Yoshida in view of Henson disclose the electronic device of claim 30, as cite above. Yoshida further discloses wherein the contact areas and the test areas at their edges and the conduction web on**

its top side have a multilayer insulation and passivation layer (figure 16 of Yoshida shows layers 4 and 5 are at the edges of the contact and test areas and on the top side of the conduction web), **and wherein the multilayer insulation and passivation layer includes a silicon dioxide layer arranged directly on the edges of the contact areas and of the test areas and on the connecting conduction web** (layers 4 and 5 is directly arranged at the edges of the contact and test areas, which includes silicon dioxide, as disclosed in col. 6, lines 2 and 13).

e. Regarding claim 32, **Yoshida in view of Henson disclose the semiconductor chip of claims 30, as cited above. Yoshida is silent with respect to the multilayer insulation and passivation layer comprises a silicon nitride layer and a polyimide layer. Henson further discloses that a multilayer insulation and passivation layer may comprise silicon nitride and a polyimide layer** (e.g. figure 7 shows multilayer insulation and passivation layers 722 and 724. col. 4, lines 22 - 23 disclose that layer 722 may be silicon oxynitride, which comprises silicon nitride, and col. 4, lines 52 – 53 discloses that layer 24 may be a polyimide layer).

It would have been obvious for one of ordinary skill in the art at the time the invention was made to use polyimide and silicon nitride for the materials of the multilayer insulation and passivation layer for the device of Yoshida since it was well-known in the art that such materials for layers can be used in test

circuits for integrated circuits, as disclosed by Henson. Furthermore, it has been held by the courts that selection of a prior art material on the basis of its suitability for its intended purpose is within the level of ordinary skill. *In re Leshing*, 125 USPQ 416 (CCPA 1960) and *Sinclair & Carroll Co. v. Interchemical Corp.*, 65 USPQ 297 (1945). One would have been motivated to use silicon nitride and a polyimide as layers in a multilayer insulation and passivation layer since silicon nitride has well known properties of insulation and is easily manufactured, and polyimide layers are thermally stable and chemically resistant.

Response to Arguments

9. Applicant's arguments with respect to claims 18, 28, 38, and 39 filed July 24, 2008 have been fully considered but they are not persuasive.

a. With respect to claims 18, 38, and 39, the applicant argues that the Yoshida reference teaches away from the claimed invention, however the Examiner respectfully reminds the applicant that arguments that alleged anticipatory prior art teaches away from the claimed invention is not germane to a rejection under section 102. See MPEP 2131.05. One may consider the “test areas” and the “contact areas” of Yoshida as being interchangeable terms, as well as being physically interchangeable in function. One may use either area as a contact area or a test area. Furthermore, while features of an apparatus may be recited either structurally or functionally, claims directed to an apparatus must be distinguished from the prior art in terms of structure rather than function. In re

Schreiber, 128 F.3d 1473, 1477-78, 44 USPQ2d 1429, 1431-32 (Fed. Cir. 1997). See MPEP 2114.

b. With respect to claim 28, the applicant argues that the Yoshida reference teaches away from the claimed invention, and that the "contact areas" and "test areas" of Yoshida are in complete contrast to the claimed invention. However, one may consider the “test areas” and the “contact areas” of Yoshida as being interchangeable terms, as well as being physically interchangeable in function. One may use either area as a contact area or a test area. Furthermore, while features of an apparatus may be recited either structurally or functionally, claims directed to an apparatus must be distinguished from the prior art in terms of structure rather than function. In re Schreiber, 128 F.3d 1473, 1477-78, 44 USPQ2d 1429, 1431-32 (Fed. Cir. 1997). See MPEP 2114.

Conclusion

10. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to ROBERT HUBER whose telephone number is (571)270-3899. The examiner can normally be reached on Monday - Thursday (9am - 6pm EST).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thao Le can be reached on (571) 272-1708. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Lex Malsawma/
Primary Examiner, Art Unit 2892

/Robert Huber/
Examiner, Art Unit 2892
October 24, 2008